IN THE CLAIMS

1. (Original) A semiconductor device, comprising:

a doped buried layer located over a doped substrate;

a doped epitaxial layer located over the doped buried layer;

a first doped lattice matching layer located between the doped substrate and the doped buried layer; and

a second doped lattice matching layer located between the doped buried layer and the doped epitaxial layer.

2. (Original) The semiconductor device as recited in Claim 1 wherein dopant concentrations of the first and second doped lattice matching layers are each less than a dopant concentration of the doped buried layer.

3. (Original) The semiconductor device as recited in Claim 2 wherein a dopant concentration of the doped substrate is less than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the doped epitaxial layer is less than the dopant concentration of the second doped lattice matching layer.

4. (Original) The semiconductor device as recited in Claim 2 further including a third doped lattice matching layer located between the first doped lattice matching layer and the doped buried layer and a fourth doped lattice matching layer located between the second doped lattice matching layer and the doped buried layer.

5. (Original) The semiconductor device as recited in Claim 4 wherein a dopant concentration of the third doped lattice matching layer is more than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the fourth doped lattice matching layer is more than the dopant concentration of the second doped lattice matching layer.

6. (Original) The semiconductor device as recited in Claim 3 wherein the dopant concentration of the doped substrate ranges from about 1E14 atoms/cm^3 to about 1E15 atoms/cm^3, the dopant concentrations of the doped buried layer ranges from about 1E19 atoms/cm^3 to about 1E20 atoms/cm^3, and the dopant concentration of each of the first and second doped lattice matching layers ranges from about 1E15 atoms/cm^3 to about 1E19 atoms/cm^3.

7. (Original) The semiconductor device as recited in Claim 1 wherein the first and second doped lattice matching layers each include a dopant gradient wherein a dopant concentration of each of the dopant gradients is greater adjacent the doped buried layer.

Claims 8-16 (Canceled)

17. (Original) A integrated circuit, comprising:

a doped buried layer located over a doped substrate;

a doped epitaxial layer located over the doped buried layer;

a first doped lattice matching layer located between the doped substrate and the doped buried layer; and

a second doped lattice matching layer located between the doped buried layer and the doped epitaxial layer;

transistors located over the doped epitaxial layer; and

interconnects located within interlevel dielectric layers located over the transistors, which connect the transistors to form an operational integrated circuit.

18. (Original) The integrated circuit as recited in Claim 17 wherein dopant concentrations of the first and second doped lattice matching layers are each less than a dopant concentration of the doped buried layer.

19. (Original) The integrated circuit as recited in Claim 18 wherein a dopant concentration of the doped substrate is less than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the doped epitaxial layer is less than the dopant concentration of the second doped lattice matching layer.

20. (Original) The integrated circuit as recited in Claim 17 further including additional active and passive devices.

Claims 21-40 (Canceled)